CLAIMS

1. A digital radio frequency (RF) transceiver circuit (100), comprising:
circuitry (110, 112, 114, 116) that is adapted to select between a transmitter input signal (148) and a receiver input signal (43);
a plurality of filters (126, 128, 130, 132) that are adapted to receive either the transmitter input signal (148) or the receiver input signal (43) and to produce either a filtered transmitter signal or a filtered receiver signal;
circuitry (138, 140, 142) that alternatively receives the filtered transmitter signal or the filtered receiver signal and produces a modulated output and a demodulated output.

2. The RF transceiver circuit (100) set forth in claim 1. wherein the plurality of filters (126, 128, 130, 132) comprises four filters that employ impulse response characteristics set forth below:

	1	z^{-1}	z^{-2}	z^{-3}	z^{-4}	z^{-5}	z^{-6}	z^{-7}	z^{-8}	z^{-9}	z^{-10}	z^{-11}
FLTR0	0	-4	7	-9	12	-12	268	-12	12	-9	7	-4
FLTR1	1	0	2	-8	19	-65	-238	50	-28	16	-10	5
FLTR2	3	-6	12	-24	47	-160	-160	47	-24	12	-6	3
FLTR3	-5	10	-16	28	-50	238	65	-19	8	-2	0	-1

3. The RF transceiver circuit (100) set forth in claim 1, wherein the plurality of filters (126, 128, 130, 132) comprise finite impulse response (FIR) filters.

4. The RF transceiver circuit (100) set forth in claim 3, wherein the plurality of filters (126, 128, 130, 132) comprises four filters that employ tap coefficient values set forth below:

	1	z^{-1}	z^{-2}	z^{-3}	z^{-4}	z^{-5}	z^{-6}	z^{-7}	z^{-8}	z^{-9}	z^{-10}	z^{-11}
FLTR0	0	-4	7	-9	12	-12	268	-12	12	-9	7	-4
FLTR1	1	0	2	-8	19	-65	-238	50	-28	16	-10	5
FLTR2	3	-6	12	-24	47	-160	-160	47	-24	12	-6	3
FLTR3	-5	10	-16	28	-50	238	65	-19	8	-2	0	-1

5. The RF transceiver circuit (100) set forth in claim 1, wherein the RF transceiver circuit comprises a portion of an orthogonal frequency division multiplexing (OFDM) transceiver (10).

6. The RF transceiver circuit (100) set forth in claim 1, wherein outputs from at least a portion of the plurality of filters (126, 128, 130, 132) are delivered as inputs to a multiplexer (142) that provides the modulated output.

7. The RF transceiver circuit (100) set forth in claim 1, wherein the modulated output is processed by a digital-to-analog (D/A) converter (32) at a frequency four times greater than a frequency of a carrier of the modulated output.

8. The RF transceiver circuit (100) set forth in claim 1, wherein the receiver input signal (43) is processed with a delay line (102, 104, 106, 108) having a plurality of output delays, each of the output delays corresponding to one of the plurality of filters and wherein each of the plurality of filters has a different delay characteristic that compensates the associated output delay.

9. A digital radio frequency (RF) transceiver circuit (100), comprising:
means for selecting (110, 112, 114, 116) between a transmitter input signal (148) and a receiver input signal (43);
means for receiving (126, 128, 130, 132) either the transmitter input signal or the receiver input signal and for producing either a transmitter signal or a receiver signal;
means for alternatively receiving (138, 140, 142) the transmitter signal or the receiver signal and for producing a modulated output and a demodulated output.

10. The RF transceiver circuit (100) set forth in claim 9. wherein the means for receiving (126, 128, 130, 132) either the transmitter input signal or the receiver input signal and for producing either a transmitter signal or a receiver signal comprises four filters that employ impulse response characteristics set forth below:

	1	z^{-1}	z^{-2}	z^{-3}	z^{-4}	z^{-5}	z^{-6}	z^{-7}	z^{-8}	z^{-9}	z^{-10}	z^{-11}
FLTR0	0	-4	7	-9	12	-12	268	-12	12	-9	7	-4
FLTR1	1	0	2	-8	19	-65	-238	50	-28	16	-10	5
FLTR2	3	-6	12	-24	47	-160	-160	47	-24	12	-6	3
FLTR3	-5	10	-16	28	-50	238	65	-19	8	-2	0	-1

11. The RF transceiver circuit (100) set forth in claim 9, wherein the means for receiving (126, 128, 130, 132) either the transmitter input signal or the receiver input signal and for producing either a transmitter signal or a receiver signal plurality of filters comprise a plurality of finite impulse response (FIR) filters.

12. The RF transceiver circuit (100) set forth in claim 11, wherein the plurality of FIR filters comprises four FIR filters that employ tap coefficient values set forth below:

	1	z^{-1}	z^{-2}	z^{-3}	z^{-4}	z^{-5}	z^{-6}	z^{-7}	z^{-8}	z^{-9}	z^{-10}	z^{-11}
FLTR0	0	-4	7	-9	12	-12	268	-12	12	-9	7	-4
FLTR1	1	0	2	-8	19	-65	-238	50	-28	16	-10	5
FLTR2	3	-6	12	-24	47	-160	-160	47	-24	12	-6	3
FLTR3	-5	10	-16	28	-50	238	65	-19	8	-2	0	-1

13. The RF transceiver circuit (100) set forth in claim 9, wherein the RF transceiver circuit comprises a portion of an orthogonal frequency division multiplexing (OFDM) transceiver (10).

14. The RF transceiver circuit (100) set forth in claim 9, wherein the means for alternatively receiving (138, 140, 142) the transmitter signal or the receiver signal and for producing a modulated output and a demodulated output comprises a multiplexer (142) that provides the modulated output.

15. The RF transceiver circuit (100) set forth in claim 9, wherein the modulated output is processed by a digital-to-analog (D/A) converter (32) at a frequency four times greater than a frequency of a carrier of the modulated output.

16. The RF transceiver circuit (100) set forth in claim 9, wherein the means for receiving (126, 128, 130, 132) either the transmitter input signal or the receiver input signal and for producing either a transmitter signal or a receiver signal comprises a plurality of filters and wherein the receiver input signal (43) is processed with a delay line (102, 104, 106, 108) having a plurality of output delays, each of the output delays corresponding to one of the plurality of filters and wherein each of the plurality of filters has a different delay characteristic that compensates the associated output delay.

17. A method of processing signals in a digital radio frequency (RF) transceiver circuit (100), the method comprising:

selecting between a transmitter input signal (148) and a receiver input signal (43);

receiving either the transmitter input signal (148) or the receiver input signal (43) and to producing either a filtered transmitter signal or a filtered receiver signal;

alternatively receiving the filtered transmitter signal or the filtered receiver signal and producing a modulated output and a demodulated output.

18. The method set forth in claim 17, comprising alternatively processing the transmitter input signal (148) or the receiver input signal (43) with at least four filters that employ tap coefficient values set forth below:

	1	z^{-1}	z^{-2}	z^{-3}	z^{-4}	z^{-5}	z^{-6}	z^{-7}	z^{-8}	z^{-9}	z^{-10}	z^{-11}
FLTR0	0	-4	7	-9	12	-12	268	-12	12	-9	7	-4
FLTR1	1	0	2	-8	19	-65	-238	50	-28	16	-10	5
FLTR2	3	-6	12	-24	47	-160	-160	47	-24	12	-6	3
FLTR3	-5	10	-16	28	-50	238	65	-19	8	-2	0	-1

19. The method set forth in claim 17, comprising creating the transmitter input signal (148) and the receiver input signal (43) using an orthogonal frequency division multiplexing (OFDM) strategy.

20. The method set forth in claim 17, comprising processing the modulated output using a digital-to-analog (D/A) converter (32) at a frequency four times greater than a frequency of a carrier of the modulated output.